Server Design is Getting Complicated

Like never before, today's computing environment requires an increasing complexity of enterprise-level equipment. As data rates rise, complexity issues are exacerbated by the performance limits being encountered in standard-build materials.

Faster data rates require faster rise times, which incur more loss in high-speed signals. While higher performance laminate materials can be used to compensate, the results may not be enough and can involve a significant cost. Newer processors and motherboards are handling more and more I/O, contributing to PCB trace and layout density. In addition to PCI Express®, onboard storage applications may be trying to route high-speed SAS. The PCIe/SAS I/O signals may need to go long distance runs within a server chassis, incurring the channel length based losses. PCIe re-timers are an option, but also increase cost and complexity.

Re-timers do not provide an adequate solution for high-performance computing since they increase the latency in the signal transmission.

These competing needs contribute to congestion in a PCB design. Increasing layer count is an option, but that impacts cost, as well as performance. Decreasing trace width is not a good option, as it further shortens signal reach at a given data rate. Compensating with wider traces increases the congestion as well as presenting routing issues leading to and from fine pitch components.

What is a system architect to do?

The last several years have seen an increase in the adoption of high-speed internal cable assemblies. And industry standards are increasingly defining cable-to-board systems as a result, such as the ANSI T-10 SAS committee. SAS 4 is capable of 22.5 Gbps and has components defined to support that.

Others, such as PCI Express (PCIe) have non-specified assemblies, though those assemblies have often used SAS-type assemblies. PCIe 3.0 specifies 8GTps, but no cable assembly interconnect. PCIe 4 specifies 16GTps, and is the first of the PCIe standards to define an internal cable assembly system.

The CABLINE®-VS II Micro-Coaxial Cable Connector is a high-speed differential coax wire-to-board connector system, ideal for the performance and mechanical demands of Enterprise Computing equipment.

PCIe is used to connect the processor to SAS controllers and to other peripheral devices, such as General Purpose Graphic Processing Units (GPU). GPUs can use up to 16 lanes of PCIe (32 pairs, plus clock and grounds) and are frequently used in mission critical and/or high-performance applications. Today's enterprise servers can incorporate several GPUs into a chassis. It is not practical to attach the GPUs with PCBs, due to PCB losses and distances required for all of the system components.

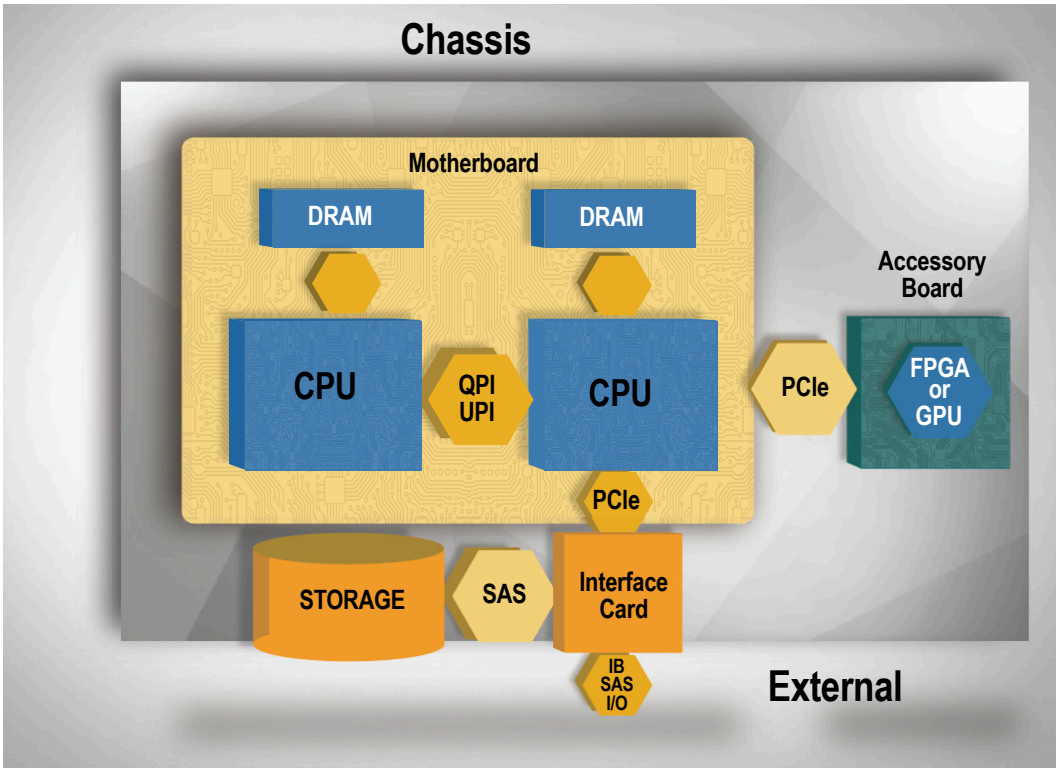
4.0 Basic Server Architecture

Server chasis will have motherboard with
- Processsors
- Memory

Other Frequent Options
- Accessory Board - GPU, FPGA, etc
- Interface Card
- Internal Storage (SAS or SATA)

Links are often PCB trace
- Cable is Optional and Growing

External Links are External Cable I/O



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Differential pair cable assemblies can bridge this gap, as well as provide more mechanical options for GPU placement. Placement is an important consideration, as the power consumption and heat output of systems increase with the processors and GPUs. Airflow is critical and must not be blocked. The challenge for cable assembly usage is to avoid airflow obstruction while providing the mechanical and connectivity requirements desired.

Thus, it is important to consider the mechanical criteria around cable assemblies. Low profile, low loss, density and flexibility are all desirable features. Some cable assemblies are cumbersome to route through a system, requiring generous bend radii that consume even more space. Other cable assemblies are low profile, but require elaborate folding. Many do not have full 360-degree flexibility, or they use solid conductor construction, which contributes to cable stiffness.

There is a long history of micro-coaxial assemblies being used in laptops and other devices, with speeds operating up to 20 Gbps in USB-C implementations. Co-axial wire can be differentially driven with minimal impact on signal integrity performance. Micro-coax assemblies offer excellent performance, similar to twin axial assemblies, but typically use stranded conductors, greatly enhancing flexibility. A major benefit to consider is the economies of scale that the mobile computing market provides, giving a favorable impact on the acquisition costs of the micro-coaxial assemblies.

The performance of micro-coaxial assemblies is enhanced by direct-to-contact termination. This eliminates the introduction of PCB losses as well as the additional terminations associated with PCBs. These extra sources of discontinuities and reflections can degrade signal integrity.

Cable assemblies can be constructed with the wires held in flat configurations, bundled configurations or mixed. Available connectors provide extremely low profile terminations, allowing for fully-shielded right angle launches below 2mm high, vertical-shielded terminations with latching and others.

Application scenarios have numerous possibilities including straightforward jumper assemblies that fly over the board and low profile assemblies that can route underneath the motherboard between PCB and chassis, or route between components and chassis side walls. High-temperature cable versions are also available, addressing any temperature concerns that arise in given applications allowing placement near processors.

For more information and to help determine which I-PEX Connector is compatible with your system's needs, contact your I-PEX Connectors representative or visit I-PEX Connectors online at www.i-pex.com.

The CABLINE® CA-II Micro-Coaxial Wire-to-Board Connector has full 360-degree EMI shielding allowing for greater flexibility in placement on the board.

www.i-pex.com

I-PEX® connectors