LIGHTPASS™-EOM 100G

Part No. 88001-000T-25-01

Product Specification

00	S21398	August 26, 2021	K.Nishiyama	-	Y.Hashimoto
Rev.	ECN	Date	Prepared by	Checked by	Approved by

1. Features

- 4 channel transmitter and 4 channel receiver Integrated module
- High Channel Capacity: 25Gbps x 4 Channels
- High density: 12.0 mm X 14.0 mm size.
- Low power consumption per Gbps: < 10 mW/Gbps for TX–RX pair
- 1.3-um Laser array in transmitter; PD array in receiver
- Operates up to 25.8 Gbps with 64b/66b compatible coded data (PRBS-31) (TBD)
- Links up to 300 m at 25.8 Gbps with 1.3-um optimized MMF (TBD)
- Electrical interface: Socket Connection
- Optical Interface: 12 core MT-connecter via 12 core Multi Mode Fiber
- Three power supplies, 1.0 V, 1.1 V and 3.3 V
- Controlled by quasi-I2C
  - Individual channel functions: disable / enable
  - Programmable receiver output swing
  - Cross point and MZ operating point should be controlled via I2C
- Temperature monitor
- User can select Internal LD driver and External LD driver
- 0 to 85 degC case temperature operating range (TBD)

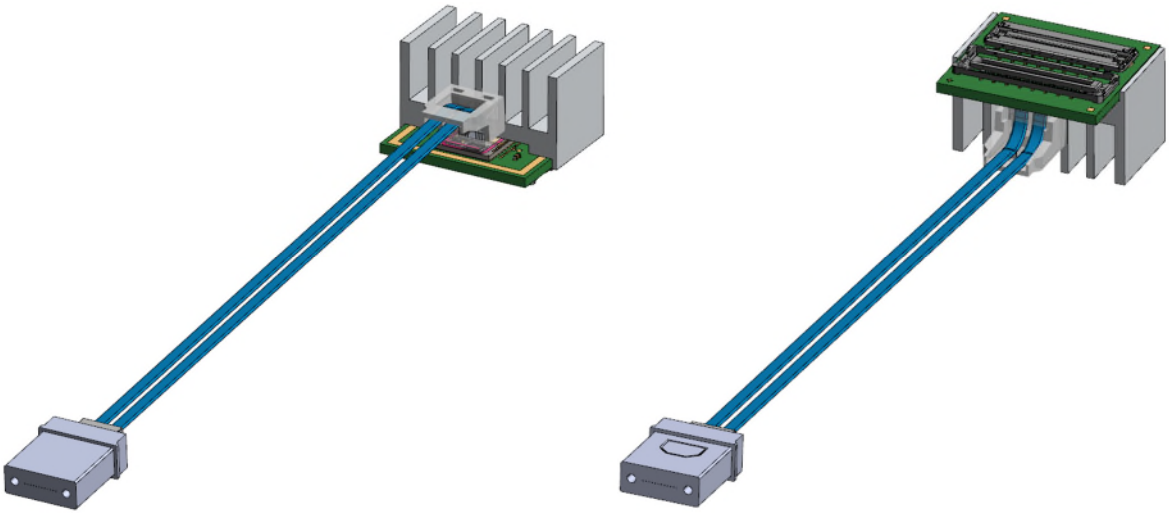


Figure 1. Figure of Embedded Optical I/O Core Module

2. Description

The TRX (optical transmitter and Receiver, EO/OE) module is an integrated module of 4ch TX and 4ch RX. It incorporates a laser diode array, 4ch input buffer, 4ch optical modulator, control and monitor blocks, 4-channel PDs (Photo Detectors) and TIAs. In addition to this, 3-lane LD driver (LDD) is implemented. The TRX is designed as Class XX (TBD).

Input buffers are designed for CML compatible; please refer to the section “High Speed Signal Interface”.
The receiver (OE) module incorporates 4-channel PDs (Photo Detectors) and TIAs. The RX output is CML compatible, and its swing can be updated via I2C. Basically external DC blocking capacitors are required between the RX output and host SERDES input.

I2C provides users a simple control scheme. A single pair of SCL and SDA controls both EO and OE.
One analog bias voltage (VBIAS) is required. Please design PCBs to be able to supply the VBIAS voltage from 0.3V to 1.6V.

The thermal budget requires an adequate thermal design for system to maintain the module / chip temperature (Tc) to be between 0 and 65 C (TBD) during operation.

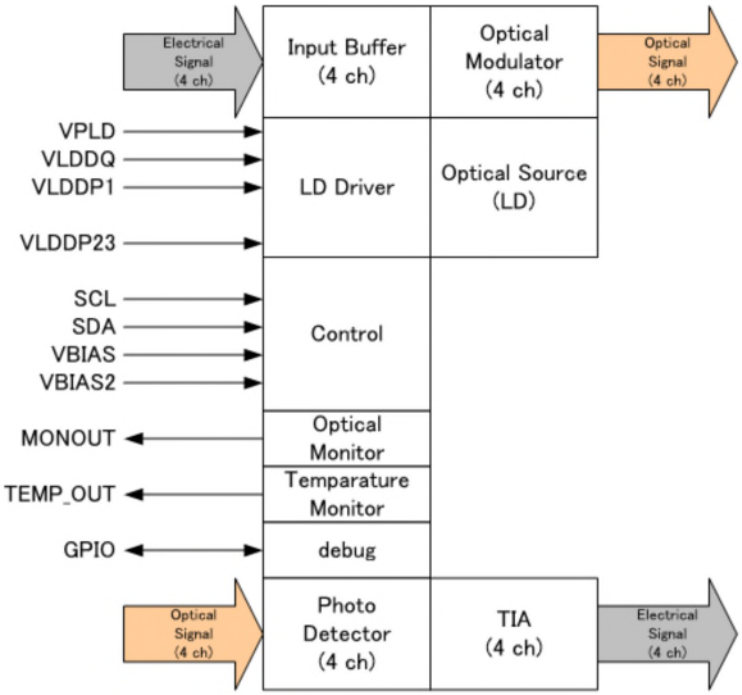


Figure 2. Transmitter / Receiver Block Diagram

3. High Speed Signal Interface

Figure 3 shows the interface between an ASIC/SerDes and the optical I/O core TX (EO) and RX (OE); only one channel is shown. DC blocking capacitors may be required in series for both TX and RX. Differential impedances are nominally100-ohm. Unused input / output pins should be terminated by 100-ohm differential loads.

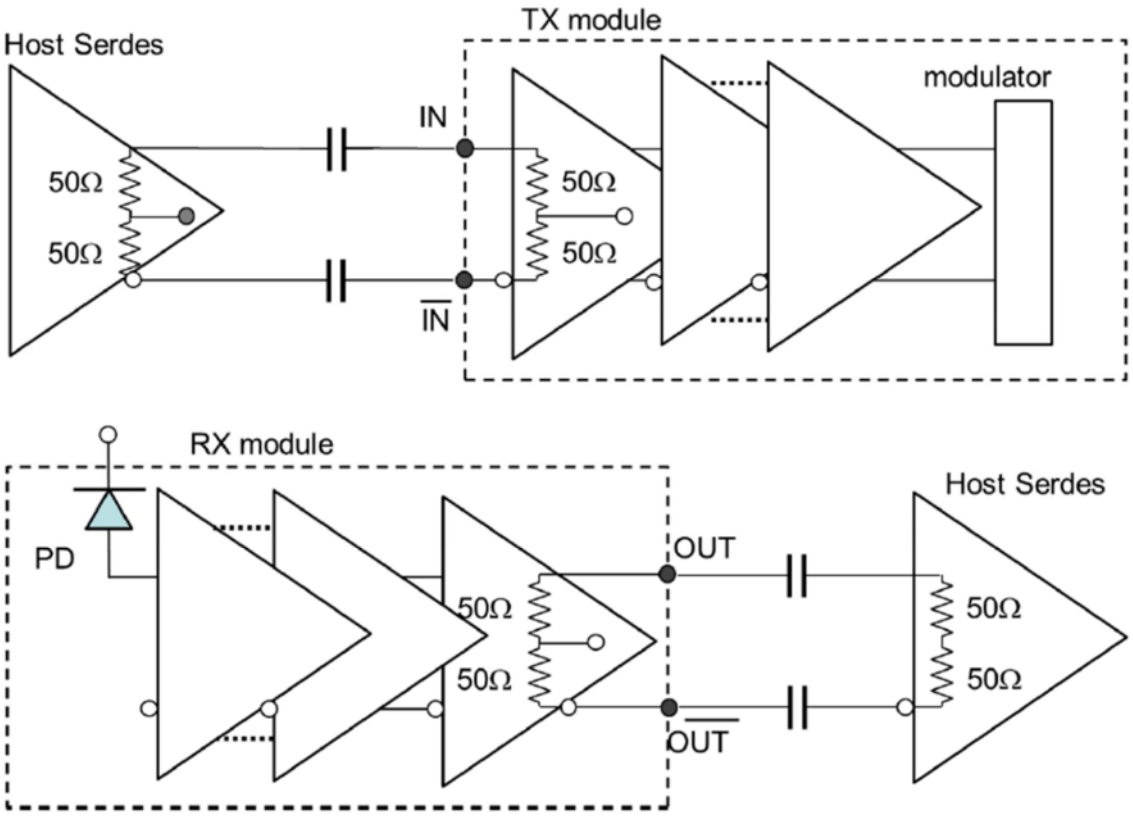


Figure 3. Interface block diagram between Host SerDes and Optical I/O core TX/RX.

4. Control Signal Interface

Optical I/O cores have quasi-I2C interface to control the operating status and it supports a slave mode. The reason why it is a “quasi”-I2C is that our SDA does not have output buffers. So, when the conventional / commercial I2C hardware is connected to our “quasi”-I2C, it may wait for the reply from the Optical I/O core and hang up. Standard I2C should have open-drain buffers, though, because our SDA does not have output buffers, SCL and SDA can be driven by one of 3.3V-open-drain and 3.3V-CMOS buffers. SCL and SDA of the quasi-I2C are designed to be 3.3V tolerant.
The registers Map is described in the section “Register Map”.

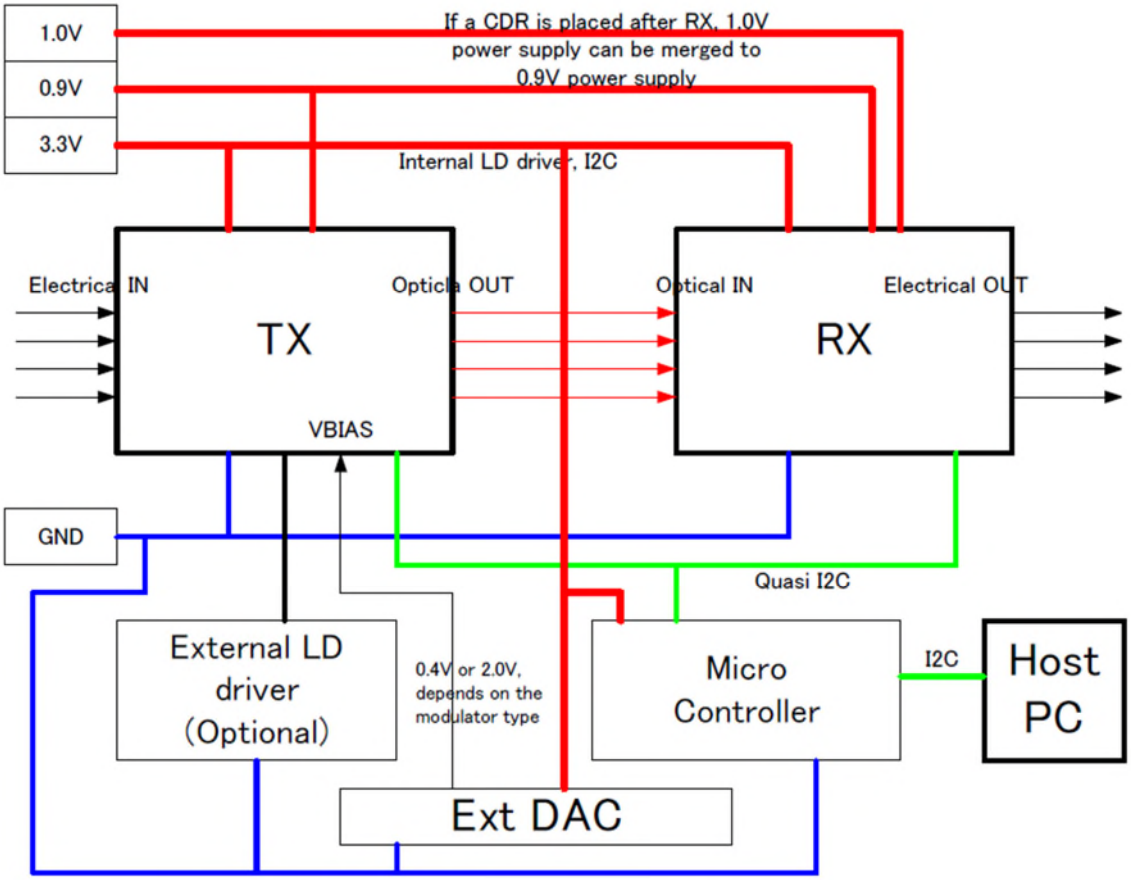
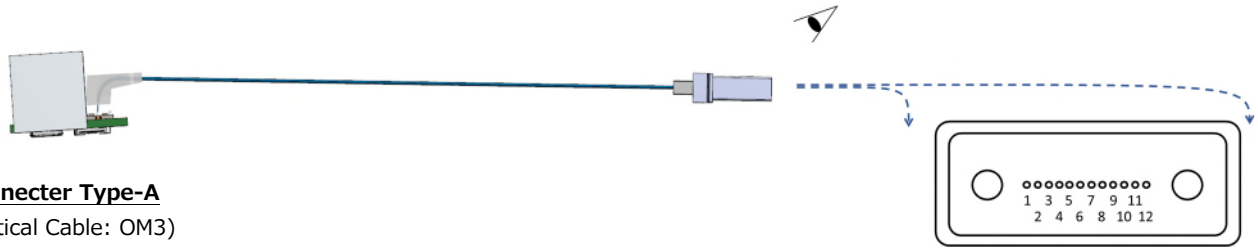


Figure 4. Block Diagram of OPTICAL I/O CORE and external circuit

5. Optical Input / Output Interface

Embedded optical I/O core module has 12 core optical cable (Multi Mode Fiber) and MT-connector.
As for the connecter type, please also refer Section 13.



Connecter Type-A
(Optical Cable: OM3)

#	Signal
1	No Connection
2	OPT_IN04
3	OPT_IN03
4	OPT_IN02
5	OPT_IN01
6	No Connection
7	No Connection
8	OPTOUT04
9	OPTOUT03
10	OPTOUT02
11	OPTOUT01
12	No Connection

Table 5. MT-connector Pin Assignment

6. Maximum Ratings

Even if all other parameters are within the recommended operation conditions, a stress in the parameters described below can cause a catastrophic damage to the module / chip. In addition to this, an exposure to the condition beyond this table, module / chip reliability may be affected.

Parameter	Symbol	Min	Max	Units	Ref.
Storage Temperature		-40	85	°C	
0.9 V Power Supply Voltage	VDD09 VDD09A VDD09B	-0.5	1.3	V	
1.0 V Power Supply Voltage	VDD10	-0.5	1.3	V	
3.3 V Power Supply Voltage	VDD33 VDD33_VPD ARM_VDD33	-0.5	4.0	V	
3.3 V Power Supply Voltage for PD (Photo Detector)	VPD	-0.5	4.0	V	
3.3 V Power Supply Voltage for LD (Laser Diode)	VLDDP[1-3] VLDDQ VPLD	-0.5	4.0	V	
Data Input Voltage – Single Ended	DI0n DIN0n (n=1-4)	VDD09 -0.7	VDD09 +0.1	V	
Data Input Voltage – Differential	|DI0n – DIN0n| (n=1-4)	0.2	0.8	V	
Control Input Voltage (quasi-I2C)	SCL SDA	-0.5	VDD33+ 0.5 4.0	V	
Bias Voltage VBIAS	VBIAS	0.1 V - 2.5 V , depends on the lot of Optical I/O Core			
Bias Voltage VBIAS2	VBIAS2	Connect to GND33 by low impedance			
Analog Input / Output Port for Debug	GPIO	-0.5	4.0	V	
Monitor output	MONOUT TEMP_OUT	Please monitor the voltage of this node by ADC. Voltage range is 0.1 V - 3.2 V			
Relative Humidity	RH	5	95	%	(*1)

7. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Case Temperature	Tc	-40		85	℃	
0.9 V Power Supply Voltage	VDD09 VDD09A VDD09B	0.90	0.95	1.0	V	
1.0 V Power Supply Voltage	VDD10	1.0	1.05	1.2	V	
3.3 V Power Supply Voltage	VDD33 T_VDD33 R_VDD33	3.135	3.3	3.465	V	
Signal Rate per Channel (rates < 3.125 Gbps must be 8b/10b encoded)	B	1.0		25.8	Gbps	
Data Input Differential Peak-to-Peak Voltage Swing		200		800	mV	
Data Input Common Mode Voltage		0		VDD33	V	
Data Input Rise & Fall Times (20% - 80%)				35	ps	
Data Input Deterministic Jitter , 25.8Gbps				6	ps	
Data Input Total Jitter , 25.8Gbps				12	ps	
I2C Interface Clock Rate				300	kHz	
I2C Interface Write Cycle Time	twc	40			ms	
Power Supply Noise			5%		mV p-p	
Receiver Differential Data Output Load			100		Ohms	
AC Coupling Capacitors - Receiver Data Outputs			0.1		µF	
Fiber Length: 2000 MHz・km 50µm MMF		0.5		300	m	

8. Transmitter Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions.
Typical values are for Tc = 40 °C, VDD33 = 3.3-V, VDD10 = 1.0-V and VDD09 / VDD09A / VDD09B = 0.9-V.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Power Consumption					W	When Internal LDD is not used
Power Supply Current - VDD09 (25 degC)			91.7		mA	(per channel)
Power Supply Current - VDD09 (85 degC)				170	mA	(per channel)
Power Supply Current - VDD33			7	8	mA	
Eye Opening in Data Input Voltage (differential)		200		1200	mV	(diff)
Differential Input Impedance			100		ohm	
Differential Input Return Loss, 10 M - 2.8 GHz	Sdd11		18		dB	@2.8GHz(Sim)
Differential Return Loss, 2.8 G -12.5 GHz	Sdd11		9.5		dB	@12.5GHz(Sim)
Common Mode Input Return Loss, 2.5 G - 28 GHz	Scc11		TBD		dB	
LOS Assert Threshold: TX Data Input Differential Peak-to-Peak			TBD		mVpp	
Power On Initialization Time			TBD		ms	I2C preset values needs to be loaded. Initialization time depends on the cycle time of microcontroller.

9. Receiver Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions.
Typical values are for Tc = 40 ° C, VDD33 = 3.3-V, VDD10 = 1.0-V and VDD09 / VDD09A / VDD09B = 0.9-V.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Power Consumption			0.088		W	(per channel)
Power Supply Current - VDD09A (25 degC)			9.6		mA	(per channel)
Power Supply Current - VDD09A (85 degC)				TBD	mA	(per channel)
Power Supply Current - VDD09B (25 degC)			58		mA	(per channel)
Power Supply Current - VDD09B (85 degC)				110	mA	(per channel)
Power Supply Current - VDD10 (25 degC)			27.7		mA	(per channel)
Power Supply Current - VDD10 (85 degC)				35	mA	(per channel)
Power Supply Current - VDD33			0.96		mA	
Data Output Differential Peak-to-Peak Voltage Swing			670		mVpp	(Eye Height)
Data Output Common Mode Voltage			833		mV	
Output Rise/Fall time (20-80%)			16/14		ps	
Receiver BW			13		GHz	
Differential Output Impedance			100		ohm	
Differential Output Return Loss, 10M- 2.8GHz	Sdd22		16		dB	
Differential Output Return Loss, 2.8GHz – 12.5 GHz	Sdd22		13.5		dB	
Low Frequency Cut-off				100	kHz	
CM to Differential Mode Conversion, 0.1G- 11.1GHz					dB	
Power On Initialization Time					ms	An initialize sequence via I2C setting is required.
Inter-channel Skew				(7)	ps	TBD

10. Transmitter Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions.
Typical values are for Tc = 40°C, VDD33 = 3.3-V, VDD10 = 1.0-V and VDD09 / VDD09A / VDD09B = 0.9-V.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Output Optical Power: Average		0		3.0	dBm	
Output Optical Power: Disabled				-15	dBm	
Extinction Ratio		3			dB	
Encircled Flux	meets 100 GBASE-SR10. Measured data can be disclosed.					
Center Wavelength			1310		nm	depending on temperature
Spectral Width - rms			3		nm	
Accumulated Deterministic Jitter					ps	TBD
Accumulated Total Jitter					ps	TBD

11. Receiver Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions.
Typical values are for Tc = 40˚C, VDD33 = 3.3 V and VDD10 = 1.0V

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Input Optical Power Sensitivity in OMA			-6.0	(-5.0)	dBm	
Operating Center Wavelength		1280		1350	nm	depending on temperature
Return Loss				-10	dB	

12. Mechanical Outline

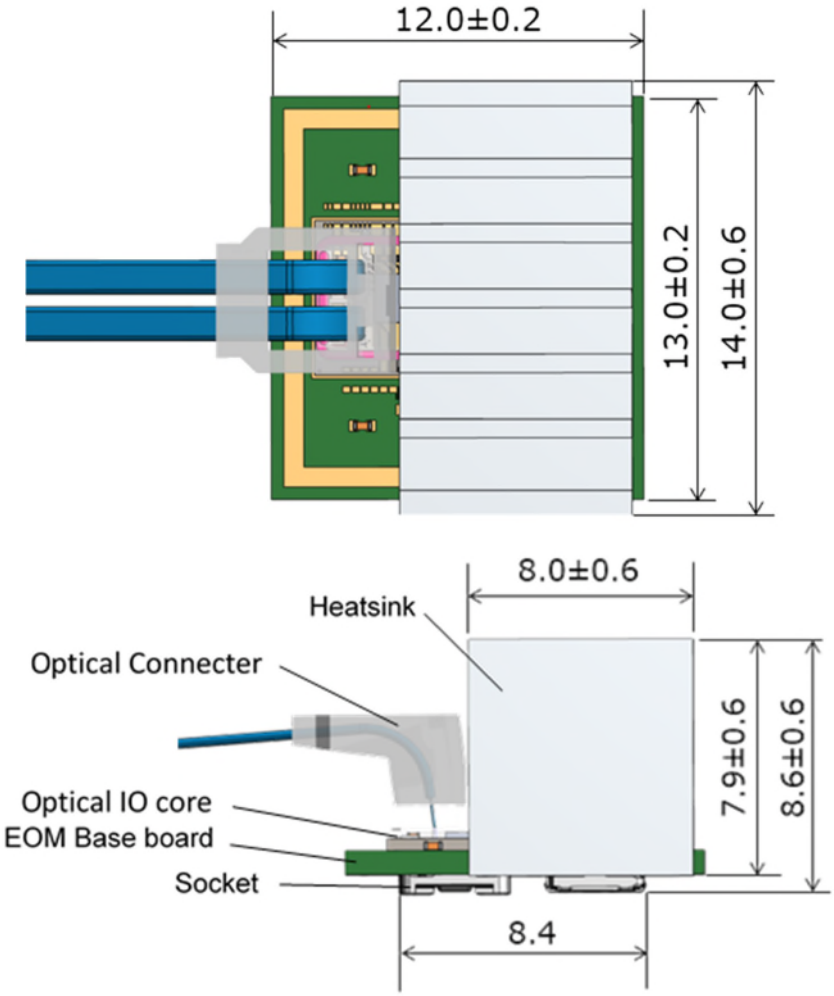


Figure 12. Mechanical Dimensions

13. Pin Assignment

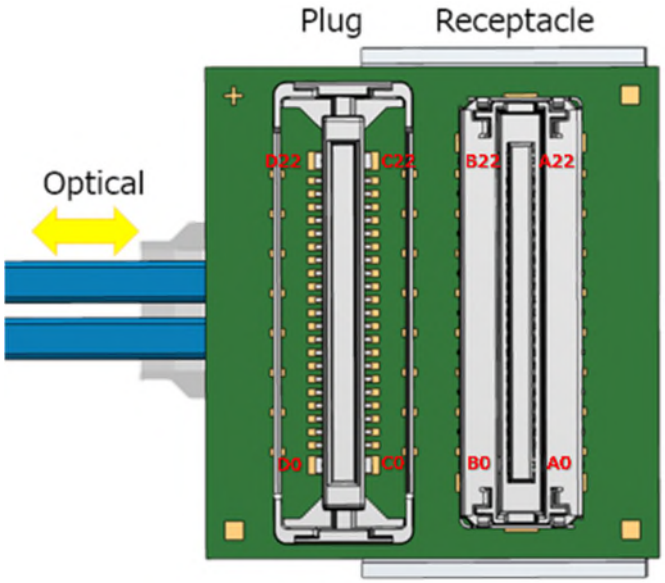


Figure 13. Pin Coordination of Embedded IO Core (Socket pin)

Plug				Receptacle			
D22	VLDDQ	C22	VLDDQ	B22	GND-TX	A22	GND-TX
D21	VLDDP3	C21	TEMP_OUT	B21	GND-TX	A21	GND-TX
D20	VLDDP2	C20	TVDD33	B20	GND-TX	A20	DI01
D19	VLDDP1	C19	GND-TX	B19	GND-TX	A19	DIN01
D18	GND-TX	C18	GND-TX	B18	DI02	A18	GND-TX
D17	VDD09	C17	VPLD	B17	DIN02	A17	GND-TX
D16	VDD09	C16	VPLD	B16	GND-TX	A16	DI03
D15	VDD09	C15	VPLD	B15	GND-TX	A15	DIN03
D14	VDD09	C14	VPLD	B14	DI04	A14	GND-TX
D13	GND-TX	C13	GND-TX	B13	DIN04	A13	GND-TX
D12	GND-TX	C12	GND-TX	B12	GND-TX	A12	GND-TX
D11	GND-ETC	C11	GND-TX	B11	GND-TX	A11	GND-ETC
D10	VBIAS2	C10	GND-ETC	B10	GND-ETC	A10	GND-ETC
D9	MONOUT	C9	GND-ETC	B9	GND-ETC	A9	OM01
D8	GPIO	C8	GND-ETC	B8	GND-ETC	A8	OP01
D7	SCL	C7	VBIAS	B7	OM02	A7	GND-ETC
D6	SDA	C6	GND-ETC	B6	OP02	A6	GND-ETC
D5	RVDD33	C5	VDD10	B5	GND-ETC	A5	OM03
D4	GND-ETC	C4	VDD10	B4	GND-ETC	A4	OP03
D3	VDD09A	C3	VDD09B	B3	OM04	A3	GND-ETC
D2	VDD09A	C2	VDD09B	B2	OP04	A2	GND-ETC
D1	GND-ETC	C1	VDD09B	B1	GND-ETC	A1	GND-ETC
D0	GNDPD	C0	VPD	B0	GND-ETC	A0	GND-ETC

Table 13. Pin Assignment of Embedded IO Core (Socket pin)

14. Pin Description

Signal Name	Description	In/Out	type
DI01-04	Non-inverting Data Input for channels 01-04	In	CML
DIN01-04	Inverting Data Input for channels 01-04	In	CML
GND-TX	GND for VDD09 and T_VDD33	In	
GND-ETC	GND for VDD09A, VDD09B and VDD10	In	
GNDPD	GND for VPD	In	
GPIO	General Purpose I/O for debugging	In/Out	
MONOUT	Optical monitor output	Out	0 to 3.3V analog voltage
OM01-04	Inverting Data Output for channels 01-04	Out	CML
OP01-04	Non-inverting Data Output for channels 01-04	Out	CML
R_VDD33	3.3V power supply for quasi-I2C	In	
SCL	SCL for quasi-I2C	In	3.3V OPENDRAIN or CMOS
SDA	SDA for quasi-I2C	In	3.3V OPENDRAIN or CMOS
T_VDD33	3.3V Power supply for internal LDD controller	In	
TEMP_OUT	Temperature monitor output	Out	0 to 3.3V analog voltage
VBIAS	Analog bias voltage for optical modulator	In	1.9 - 2.1V or 0.3 - 0.5V (*1)
VBIAS2	Analog bias voltage for optical modulator	In	set to 0V by user
VDD09	0.9V power supply for TX	In	
VDD09A	0.9V power supply for RX	In	
VDD09B	0.9V power supply for RX	In	
VDD10	1.0V power supply for RX	In	
VLDDP1	LD power supply; refer to Appendix "internal and external LDD"	In	
VLDDP2	LD power supply; refer to Appendix "internal and external LDD"	In	
VLDDP3	LD power supply; refer to Appendix "internal and external LDD"	In	
VLDDQ	LD power supply; refer to Appendix "internal and external LDD"	In	
VPD	3.3V power supply for PD	In	
VPLD	LD power supply; refer to Appendix "internal and external LDD"	In	
OPT_IN01-04	Multi-mode optical signal input for channels 01-04	In	
OPTOUT01-04	Multi-mode optical signal output for channels 01-04	Out	

(*1) VBIAS voltage value depends on the type of optical modulator.

Table 14. Pin Description

15. Register Map

As for the high-speed signal interface, please refer the Optical I/O core datasheet.

Optical I/O core Datasheet: PAA-XW8001-ESB Datasheet (AIO-30-18-020-014)

16. Regulatory Compliance

Optical I/O core modules / chips are RoHS-6 Compliant (TBD).

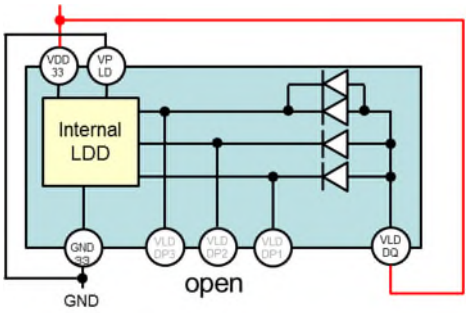
And TX modules / chips are Class 1M laser eye safety compliant per IEC 60825-1 (TBD).

17. Internal and External LD Driver

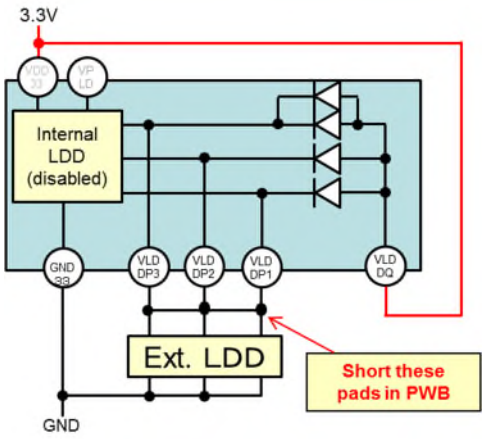
Customer can choose internal LD-driver (LDD) or external LDD for their design. When customer places external LDD, both internal LDD and external LDD drive LD are prohibited. Please make sure internal or external LDD drives LD by setting VPLD pin and internal I2C register (TRUP, Address 30H, REG_00H, bit0).

Internal LDD mode;

Connect VPLD to GND33, and connect VLDDQ to VDD33.



External LDD mode;



18. Typical Circuit

Optical IO core, Embedded Optical IO module

(Some of GND types of Optical IO core are combined to two types of GND at EOM)

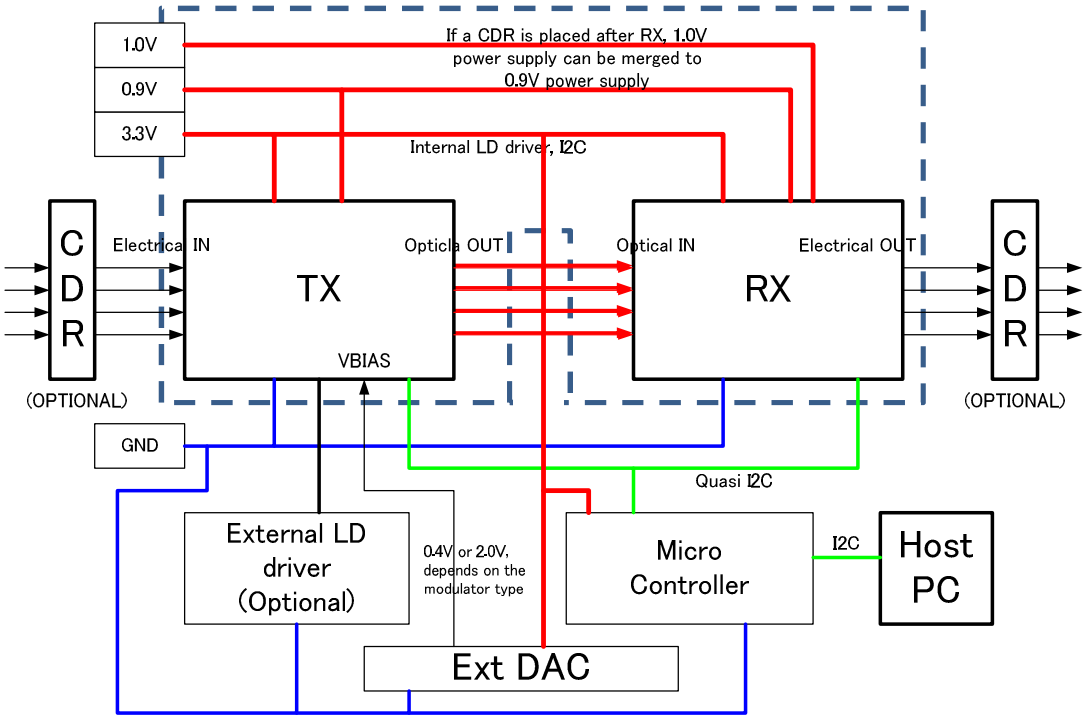


Figure 18-1. Block Diagram of OPTICAL I/O CORE and external circuit

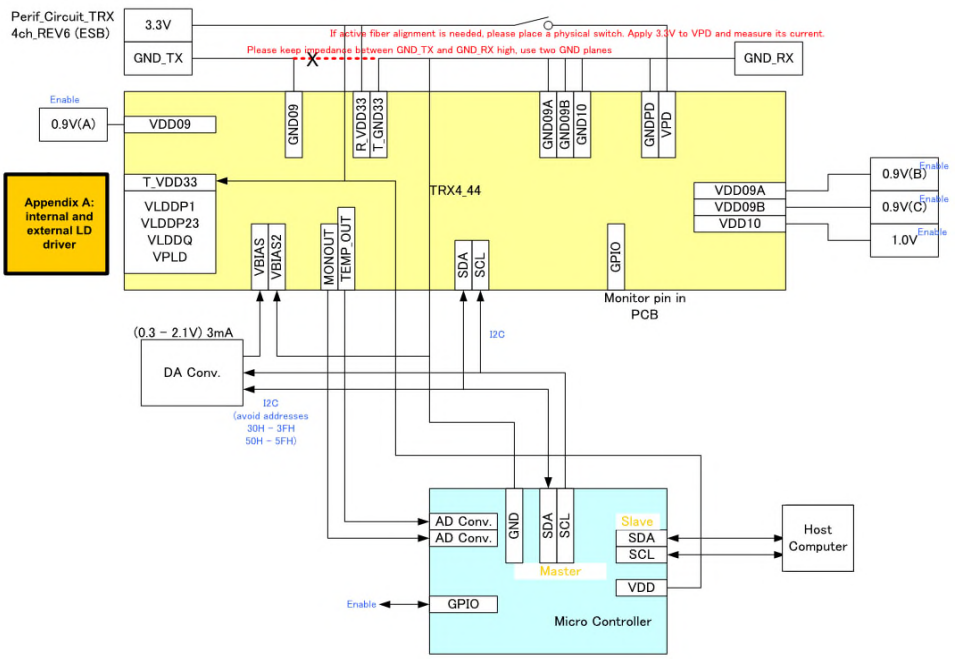
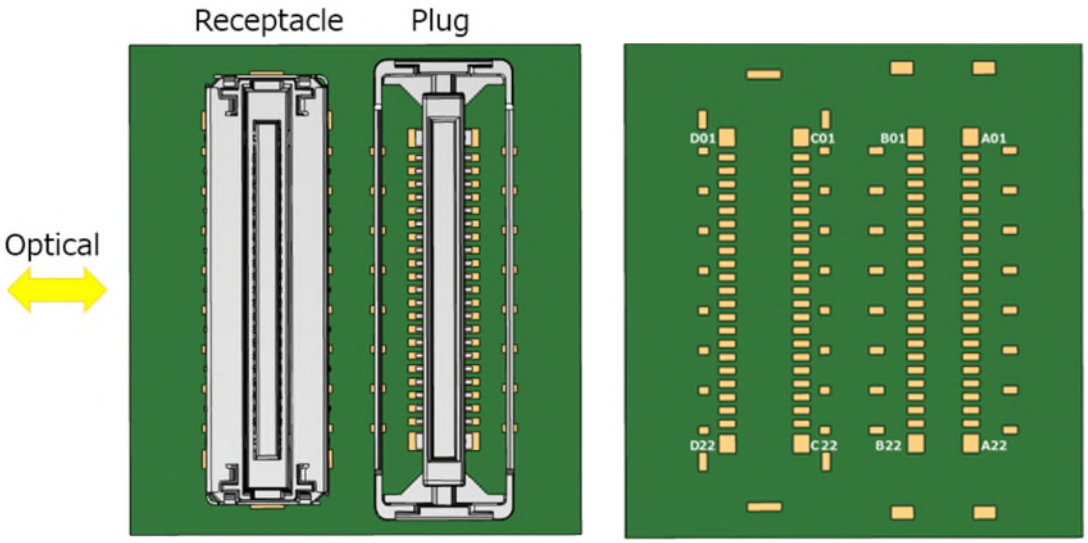


Figure 18-2. Circuit Block Diagram

19. PCB PAD Assignment

The PAD coordinates for PCB are viewed from TOP of PCB. Please refer Table 13-1 for pin assignment.



After mounting connector **Before mounting connector**

Receptacle				Plug			
D0	GNDPD	C0	VPD	B0	GND-ETC	A0	GND-ETC
D1	GND-ETC	C1	VDD09B	B1	GND-ETC	A1	GND-ETC
D2	VDD09A	C2	VDD09B	B2	OP04	A2	GND-ETC
D3	VDD09A	C3	VDD09B	B3	OM04	A3	GND-ETC
D4	GND-ETC	C4	VDD10	B4	GND-ETC	A4	OP03
D5	RVDD33	C5	VDD10	B5	GND-ETC	A5	OM03
D6	SDA	C6	GND-ETC	B6	OP02	A6	GND-ETC
D7	SCL	C7	VBIAS	B7	OM02	A7	GND-ETC
D8	GPIO	C8	GND-ETC	B8	GND-ETC	A8	OP01
D9	MONOUT	C9	GND-ETC	B9	GND-ETC	A9	OM01
D10	VBIAS2	C10	GND-ETC	B10	GND-ETC	A10	GND-ETC
D11	GND-ETC	C11	GND-TX	B11	GND-TX	A11	GND-ETC
D12	GND-TX	C12	GND-TX	B12	GND-TX	A12	GND-TX
D13	GND-TX	C13	GND-TX	B13	DIN04	A13	GND-TX
D14	VDD09	C14	VPLD	B14	DI04	A14	GND-TX
D15	VDD09	C15	VPLD	B15	GND-TX	A15	DIN03
D16	VDD09	C16	VPLD	B16	GND-TX	A16	DI03
D17	VDD09	C17	VPLD	B17	DIN02	A17	GND-TX
D18	GND-TX	C18	GND-TX	B18	DI02	A18	GND-TX
D19	VLDDP1	C19	GND-TX	B19	GND-TX	A19	DIN01
D20	VLDDP2	C20	TVDD33	B20	GND-TX	A20	DI01
D21	VLDDP3	C21	TEMP_OUT	B21	GND-TX	A21	GND-TX
D22	VLDDQ	C22	VLDDQ	B22	GND-TX	A22	GND-TX

Table 19. PAD Coordination for PCB

20. Recommended PCB Pattern Layout

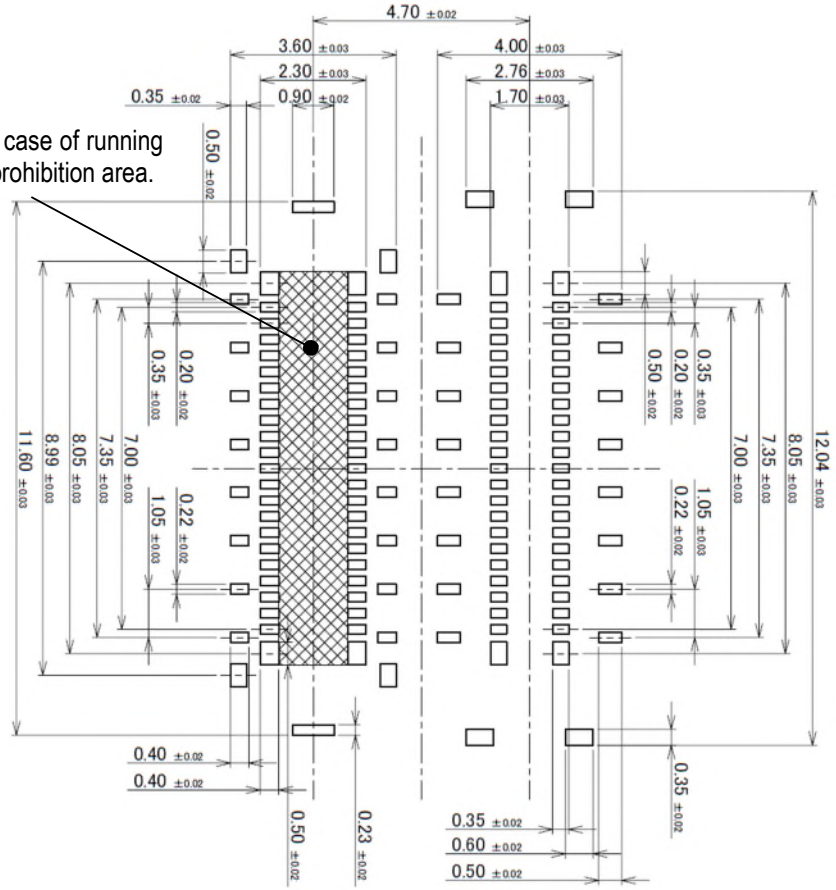


Figure 20. Recommended PCB Pattern Layout

21. Mechanical Outline (Connector)

NOVASTACK 35-HDP WITH VACUUM CAP ASS'Y

P/N 21001-042E-01

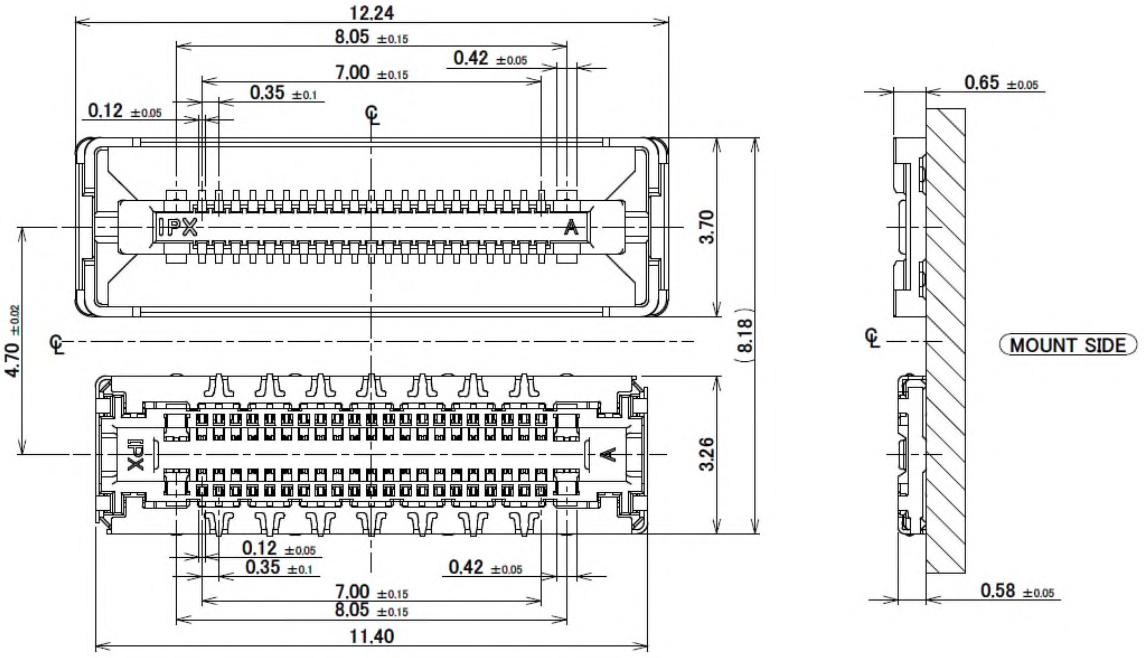


Figure 21. Mechanical Dimensions (Connector)