LIGHTPASS™-EOB 100G

Part No. 88002-000T-25-01

Product Specification

Preliminary

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Rev.	ECN	Date	Prepared by	Checked by	Approved by

1. Purpose

This product specification defines the test conditions and the performances of LIGHTPASS-EOB 100G (prototype Ver. 4C).

2. Features

- Ultra-Thin Embedded Optical Module(Mating Height: 2.3mm)
- 4 channel transmitter , 4 channel receiver and MCU integrated EOM
- High Channel Capacity: 100Gbps(25Gbps x 4 Channels)
- Operates up to 25Gbps with 1,310nm optimized MMF
- Links up to 300m at 25Gbps with 1,310nm optimized
- Electrical interface: Horizontal Connector with Mechanical Lock(CABLINE-CA/CAF®)
- Optical interface(For EXTENDED flexible choice): 12core MT Connector via 12 core Multi Mode Fiber

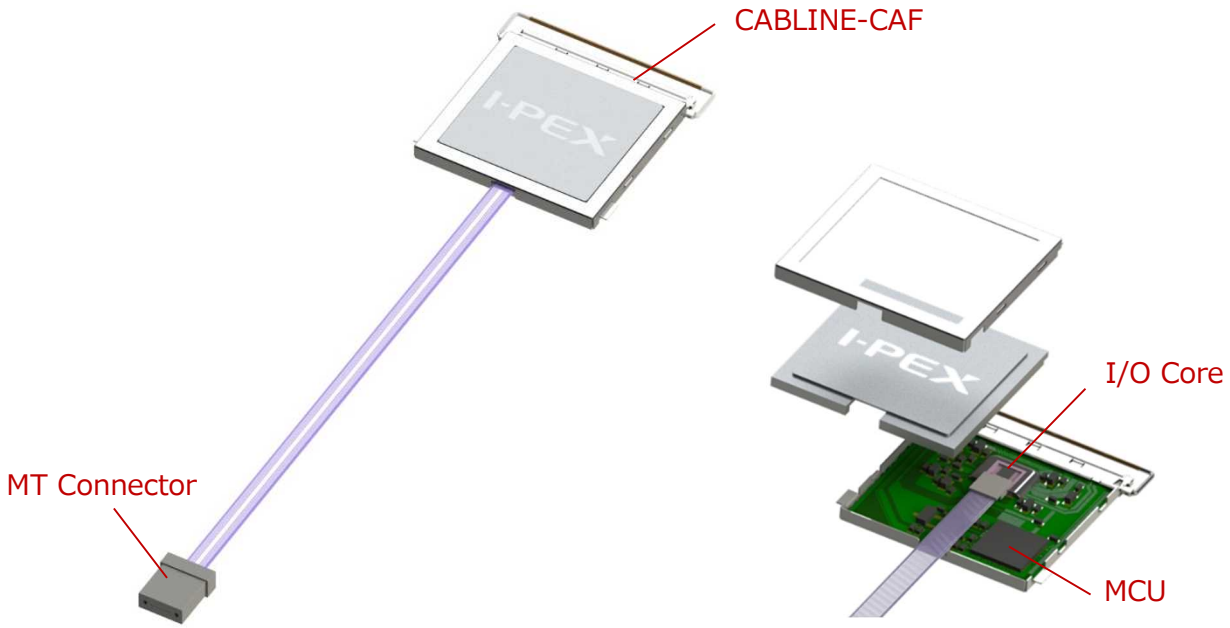

Figure 1. Figure of LIGHTPASS™-EOB 100G

3 Description

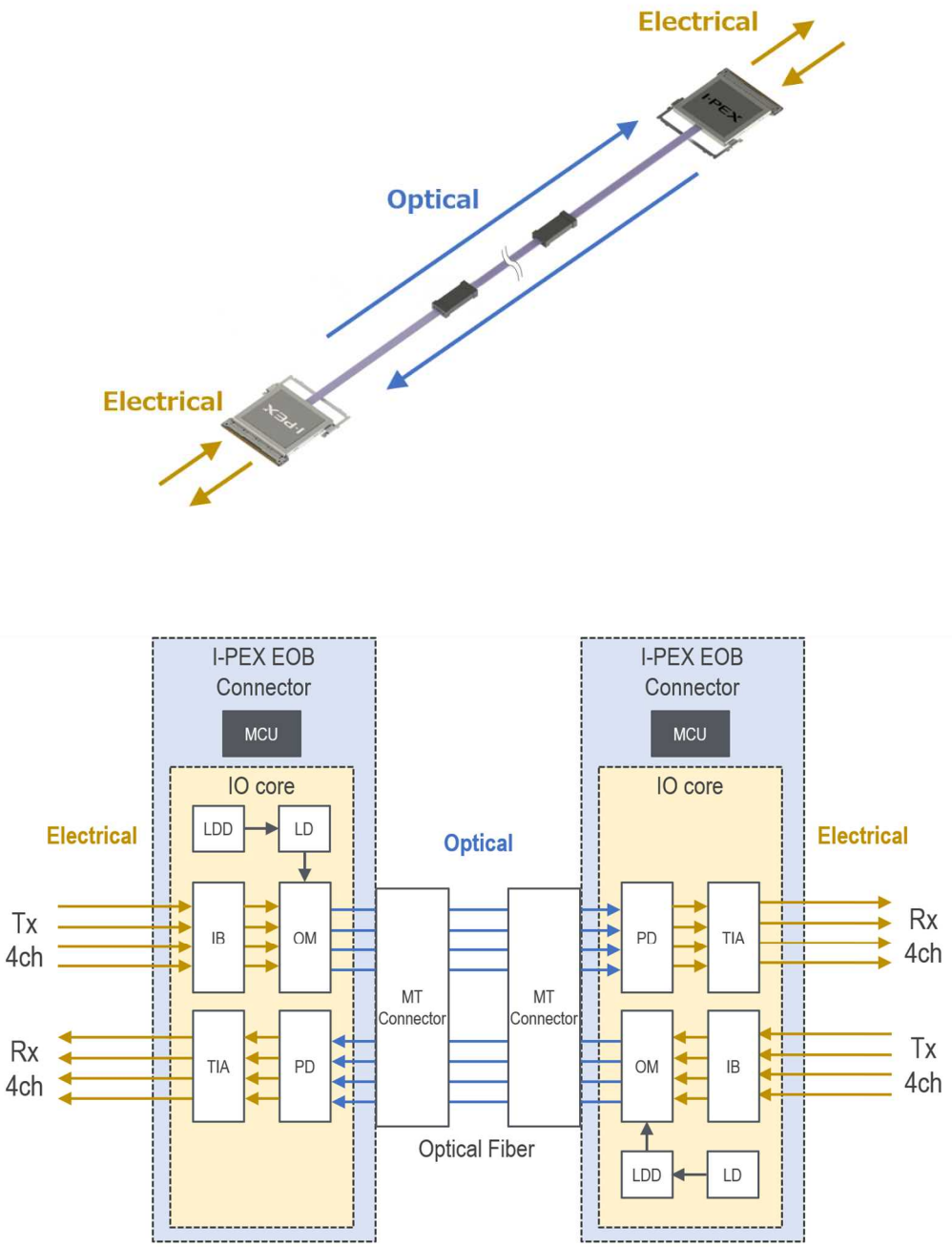

Figure 2. Transmitter / Receiver Block Diagram

4. High Speed Signal Interface

Figure 3 shows the interface between an ASIC/SerDes and the optical I/O core TX (EO) and RX (OE); only one channel is shown. DC blocking capacitors may be required in series for both TX and RX. Differential impedances are nominally100-ohm. Unused input / output pins should be terminated by 100-ohm differential loads.

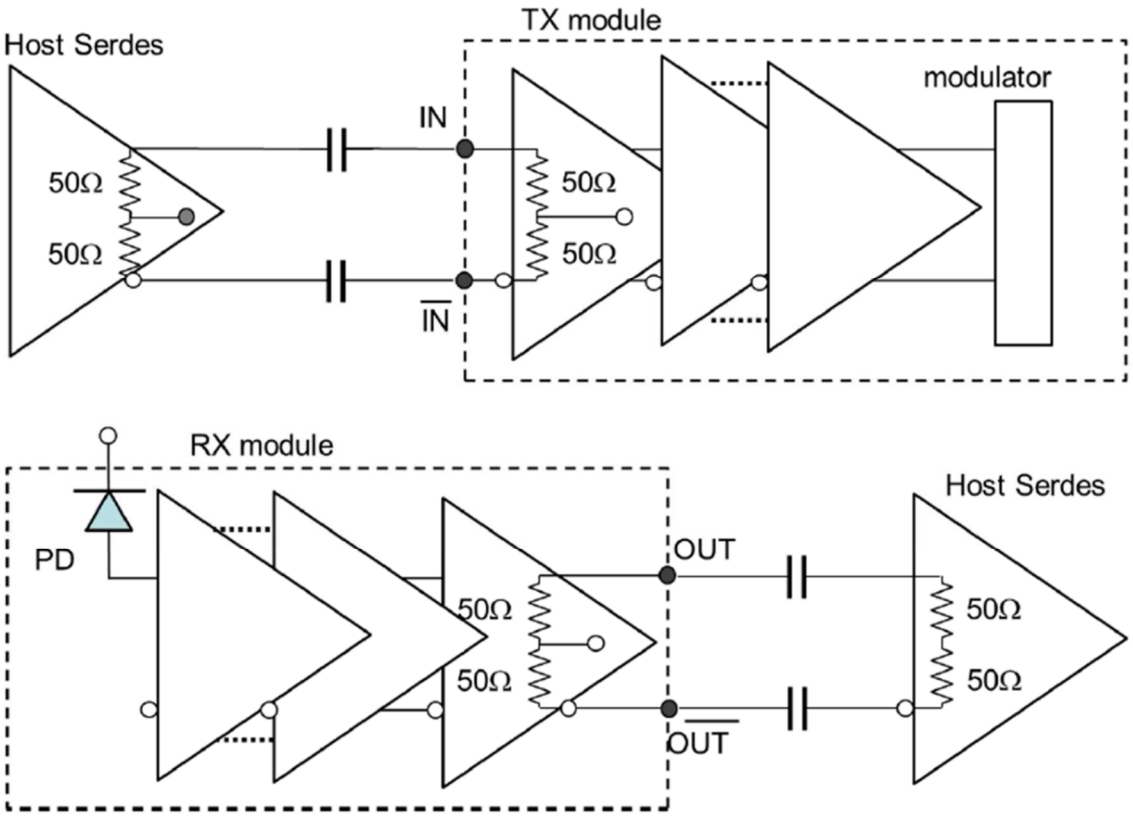

Figure 3. Interface block diagram between Host SerDes and Optical I/O core TX/RX.

5. Ratings

Even if all other parameters are within the recommended operation conditions, a stress in the parameters described below can cause a catastrophic damage to the module / chip. In addition to this, an exposure to the condition beyond this table, module / chip reliability may be affected.

Parameter	Symbol	Min	Max	Units	Ref.
Storage Temperature		-40	85	ºC	Target 105degC max.
0.9 V Power Supply Voltage	VDD09 VDD09A VDD09B	-0.5	1.3	V	
1.0 V Power Supply Voltage	VDD10	-0.5	1.3	V	
3.3 V Power Supply Voltage	VDD33 VDD33_VPD ARM_VDD33	-0.5	4.0	V	
Power Consumption (Normal)	P_act	-	3500	mW	ILD=400mA (100mA/ch)
Power Consumption (Sleep)	P_sleep	-	100	mW	TX, RX disable
VDD09 Current (Normal)	I_VDD09	-	600	mA	1.20V_typ
VDD09A Current (Normal)	I_VDD09A	-	100	mA	1.05V_typ
VDD09B Current (Normal)	I_VDD09B	-	500	mA	1.10V_typ
VDD10 Current (Normal)	I_VDD10	-	300	mA	1.20V_typ
VDD33 Current (Normal)	I_VDD33	-	30	mA	3.30V_typ
ARM33 Current (Normal)	ILD	-	15	mA	3.30V_typ
Data Input Voltage – Single Ended	TxPn TxNn (n=1-4)	VDD09 -0.7	VDD09 +0.1	V	
Data Input Voltage – Differential	|TxPn – TxNn| (n=1-4)	0.2	0.8	V	
Control Input Voltage (quasi-I2C)	I2C2_SD I2C2_SC	-0.3	4.0	V	
Relative Humidity	RH	5	95	%	(*1)

(*1) A condensing environment exposure is not allowed.

6. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Case Temperature	Tc	-40		85	℃	Fig.1 Target 105degC max.
0.9 V Power Supply Voltage	VDD09 VDD09A VDD09B	1.14 1.00 1.05	1.20 1.05 1.10	1.26 1.10 1.15	V	
1.0 V Power Supply Voltage	VDD10	1.14	1.20	1.26	V	
3.3 V Power Supply Voltage	VDD33 VDD33_VPD ARM_VDD33	3.14	3.3	3.47	V	
Signal Rate per Channel (rates < 3.125 Gbps must be 8b/10b encoded)	fdata	1.0		25.8	Gbps	
Data Input Differential Peak-to-Peak Voltage Swing	Vin	200		800	mV	(diff)
Data Input Common Mode Voltage	Vcom		720		V	
Control Input Voltage (I2C)	I2C2_SD I2C2_SC	3.14		3.47		
Data Input Rise & Fall Times (20% - 80%)	Tr/Tf			35	ps	
Data Input Deterministic Jitter , 25.8Gbps	Dj			6	ps	
Data Input Total Jitter , 25.8Gbps	Tj			12	ps	
I2C Interface Clock Rate	f_i2c	100		100	kHz	
Power Supply Noise	dV		5%		mV p-p	
Receiver Differential Data Output Load	Zout		100		Ohms	
AC Coupling Capacitors - Receiver Data Outputs	Cac		0.1		μF	
Fiber Length: OM3 50μm MMF	OM3	0.5		300	m	
Fiber Length: 2000MHz・km 50μm MMF	Corning		300		m	(*2)

(*2) By using Corning MMF optimized to 1.3um, it can be achieved.

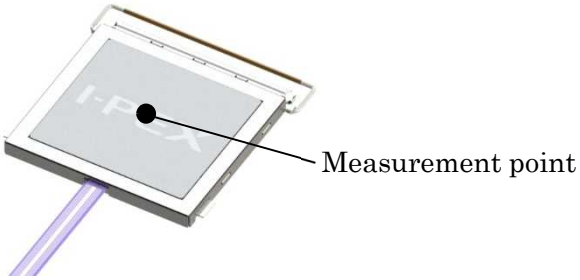

Fig.4 Case temperature

7. Transmitter Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions.
Typical values are for Tc = 40°C, VDD33 = 3.3-V, VDD10 = 1.0-V and VDD09 / VDD09A / VDD09B = 0.9-V.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Eye Opening in Data Input Voltage (differential)	Vin	200		800	mV	(diff)
Differential Input Impedance	Zdiff	80	100	120	Ohm	
Differential Input Return Loss, 10 M – 3.6GHz	Sdd11			-11	dB	at 3.6GHz
Differential Return Loss, 3.6 G -12.9 GHz	Sdd11			-6	dB	at 12.9GHz
Power On Initialization Time	Tint			500	ms	I2C preset values needs to be loaded. Initialization time depends on the cycle time of microcontroller.

8. Receiver Electrical Characteristics

The following characteristics are defined over the Recommended Operating Conditions.
Typical values are for Tc = 40°C, VDD33 = 3.3-V, VDD10 = 1.0-V and VDD09 / VDD09A / VDD09B = 0.9-V.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Data Output Differential Peak-to-Peak Voltage Swing	Vout	300	670	1000	mVpp	(Eye Height)
Data Output Common Mode Voltage	Vcm		833		mV	
Output Rise/Fall time (20-80%)	tr / tf			18/18	ps	
Receiver BW	fbw	12.9			GHz	
Differential Output Impedance	Zout	80	100	120	ohm	
Differential Output Return Loss, 10M- 3.6GHz	Sdd11			-11	dB	at 3.6GHz
Differential Output Return Loss, 3.6GHz - 12.9 GHz	Sdd11			-6	dB	at 12.9GHz
Inter-channel Skew	Tskew		7	10	ps	

9. Transmitter Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions.
Typical values are for Tc = 40 °C, VDD33 = 3.3-V, VDD10 = 1.0-V and VDD09 / VDD09A / VDD09B = 0.9-V.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Output OMA	OMA_out	-1.5			dBm	100mA/ch
Extinction Ratio	ER	3			dB	
Output Optical Power: Disabled	Pout_dis			-15	dBm	
DCOC Pave_max	Pdcoc_max	0			dBm	Pave_max in DCOC
Center Wavelength	λc	1250	1310	1350	nm	depending on temperature
Accumulated Total Jitter	Tj			13	ps	

10. Receiver Optical Characteristics

The following characteristics are defined over the Recommended Operating Conditions.
Typical values are for Tc = 40°C, VDD33 = 3.3 V and VDD10 = 1.0V

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Input Optical Power Sensitivity in OMA	OMA_in			-3.0	dBm	Link margin ⊿ = 1.5dB
Operating Center Wavelength	λc	1280		1350	nm	depending on temperature
Return Loss	RLopt			-10	dB	

11. Mechanical Outline and Pin Assign.

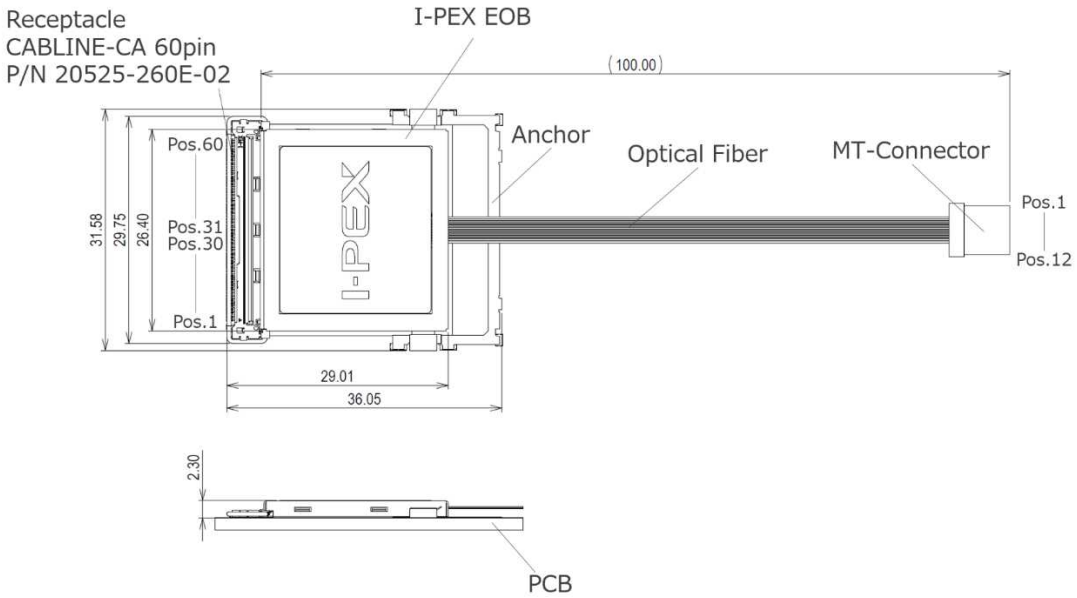

Figure 5. Mechanical Dimensions

Pos	Pin Assign
60	DGND_Rx
59	SWCLK
58	SWDIO
57	I2C2_SD
56	I2C2_SC
55	NRST
54	VPLD3
53	VPLD1
52	DCDC2_E
51	VDD09
50	VDD09
49	DCDC3_E
48	DCDC1_E
47	DGND_Rx
46	VPLD
45	VPLD
44	DGND_Tx
43	DGND_Tx
42	TxP0
41	TxN0
40	DGND_Tx
39	TxP1
38	TxN1
37	DGND_Tx
36	TxP2
35	TxN2
34	DGND_Tx
33	TxP3
32	TxN3
31	DGND_Tx

Pos	Pin Assign
30	DGND_Rx
29	RxN0
28	RxP0
27	DGND_Rx
26	RxN1
25	RxP1
24	DGND_Rx
23	RxN2
22	RxP2
21	DGND_Rx
20	RxN3
19	RxP3
18	DGND_Rx
17	DGND_Rx
16	I2C1_SC
15	I2C1_SD
14	VDD10
13	DGND_Rx
12	VDD09A
11	VDD09B
10	VDD09B
9	DGND_Rx
8	DGND_Rx
7	VDD33_VPD
6	VDD33
5	VDD33
4	DGND_Rx
3	ARM_VDD33
2	VDD50
1	DGND_Rx

CABLINE-CA Pin Assignment

Pos	Pin Assign
1	N.C.
2	Opt_out1
3	Opt_out2
4	Opt_out3
5	Opt_out4
6	N.C.
7	N.C.
8	Opt_In1
9	Opt_In2
10	Opt_In3
11	Opt_In4
12	N.C.

Type-A

Pos	Pin Assign
1	N.C.
2	N.C.
3	Opt_out1
4	Opt_out2
5	Opt_out3
6	Opt_out4
7	Opt_In1
8	Opt_In2
9	Opt_In3
10	Opt_In4
11	N.C.
12	N.C.

Type-B

MT-connector Pin Assignment

Table 1. Pin Assign

12. Pin Description

Pos	Pin Assign	Description	In/Out
60	DGND_Rx	Rx Digital GND	In/Out
59	SWCLK	MPU Debug Clock (Prototype only)	In
58	SWDIO	MPU Debug Serial (Prototype only)	In/Out
57	I2C2_SD	I2C_SD for HOST PC(Optional)	In/Out
56	I2C2_SC	I2C_SC for HOST PC(Optional)	In/Out
55	NRST	MPU Debug Reset (Prototype only)	In/Out
54	VPLD3	LD Power Supply	In
53	VPLD1	LD Power Supply	In
52	DCDC2_E	DCDC2(VDD09) Enable	Out
51	VDD09	VDD09	In
50	VDD09	VDD09	In
49	DCDC3_E	DCDC3(VDD10) Enable	Out
48	DCDC1_E	DCDC1(VDD33) Enable	Out
47	DGND_Rx	Rx Digital GND	In/Out
46	VPLD	Internal LDD GND	In
45	VPLD	Internal LDD GND	In
44	DGND_Tx	Tx Digital GND	In/Out
43	DGND_Tx	Tx Digital GND	In/Out
42	TxP0	Tx CH0_P	In
41	TxN0	Tx CH0_N	In
40	DGND_Tx	Tx Digital GND	In/Out
39	TxP1	Tx CH1_P	In
38	TxN1	Tx CH1_N	In
37	DGND_Tx	Tx Digital GND	In/Out
36	TxP2	Tx CH2_P	In
35	TxN2	Tx CH2_N	In
34	DGND_Tx	Tx Digital GND	In/Out
33	TxP3	Tx CH3_P	In
32	TxN3	Tx CH3_N	In
31	DGND_Tx	Tx Digital GND	In/Out

Pos	Pin Assign	Description	In/Out
30	DGND_Rx	Rx Digital GND	In/Out
29	RxN0	Rx CH0_N	In
28	RxP0	Rx CH0_P	In
27	DGND_Rx	Rx Digital GND	In/Out
26	RxN1	Rx CH1_N	In
25	RxP1	Rx CH1_P	In
24	DGND_Rx	Rx Digital GND	In/Out
23	RxN2	Rx CH2_N	In
22	RxP2	Rx CH2_P	In
21	DGND_Rx	Rx Digital GND	In/Out
20	RxN3	Rx CH3_N	In
19	RxP3	Rx CH3_P	In
18	DGND_Rx	Rx Digital GND	In/Out
17	DGND_Rx	Rx Digital GND	In/Out
16	I2C1_SC	I2C_SC for External LDD (Prototype only)	In/Out
15	I2C1_SD	I2C_SD for External LDD (Prototype only)	In/Out
14	VDD10	VDD10	In
13	DGND_Rx	Rx Digital GND	In/Out
12	VDD09A	VDD09A	In
11	VDD09B	VDD09B	In
10	VDD09B	VDD09B	In
9	DGND_Rx	Rx Digital GND	In/Out
8	DGND_Rx	Rx Digital GND	In/Out
7	VDD33_VPD	VDD33	In
6	VDD33	VDD33	In
5	VDD33	VDD33	In
4	DGND_Rx	Rx Digital GND	In/Out
3	ARM_VDD33	VDD33 for MPU	In
2	VDD50	VDD50 Detect (Prototype only)	In
1	DGND_Rx	Rx Digital GND	In/Out

Table 2. Pin Description